Abstract of the Disclosure:

An integrated memory has address inputs for applying a row address or a column address and a latency value, and an instruction decoder with a signal input. The instruction decoder uses a signal applied to the signal input to determine whether the address applied to the address inputs is the row address or the column address. If a column address is applied, an evaluation unit which is connected downstream of the instruction decoder and has evaluation inputs which are connected to the address inputs, is used to apply a latency signal corresponding to the latency value to an output of the evaluation unit.

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